

## Santosh Devanallikar, M.Sc., B.E.

ASIC Architecture/Design  
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### Current Role / Organization:

**Chip Architecture,  
Infinera India Pvt Ltd, Bangalore, INDIA.**

### **Summary:**

1. 22+ years of professional experience (Architecture & Chip Definition, Design & Product Development, Research, Team Management)
  - a. Analog Devices (2001-2005) – Digital Chip Design/Verification (DSP Processors)
  - b. Nvidia Graphics (2005-2006) – Digital Chip Design/Verification (Graphics/Video)
  - c. Consultant to Elven Microcircuits (Atek Infosys Pvt Ltd), Brahmashri, Prodigy labs (2007-2008) –Chip Design Leadership/Management/ Networking Software /Real time Algorithm-Software Development.
  - d. Manthan Semiconductor (2008-2009) (Worked for NXP & Ikanos Communications )
  - e. Ikanos Communications (2009-2010) Chip Design/Verification/Tech Leadership/Project Management (Networking)
  - f. Consultant to Rockwell Automation – (2011) Chip Verification (Industrial Automation)
  - g. University of Southampton, UK (2011-2012)
  - h. Consultant to Infinera Pvt Ltd (2013- 2014 - Optical Networks).
  - i. Mobiveil India Pvt Ltd (Jan-2014 to Sept-2017 – Flash & Storage)
  - j. Infinera India Pvt Ltd (Dec 2017 – Present - Optical Networking & Communications)
2. **Current focus on Architecture, Chip Definition & Requirements.**
3. Participation in 3 full chip multi-million gate SOC design Tape-Outs (Architecture to GDS-II) + 5 Complete front end Tape outs (Micro-Architecture to Net-List delivery)
4. Complete over view and understanding of ASIC methodology from Micro-architecture to GDSII
5. Hands On experience with IP Development, Chip Integration & verification
6. Experience in wide range of domains including video, networking, communications, SoC components, processors, industrial automation etc.
7. Strong understanding of Software/Hardware partitioning & development.
8. Strong understanding of Project Management including the use of tools like Microsoft project for project planning, estimation and tracking.
9. Wide exposure and skill sets in **ASIC design, FPGA flows, Software development and Web technologies.**
10. Exposure to working on inter-site projects with Israel, US and European teams.
11. **Hands-on Development (Software/Hardware), Project Management and Business Development/Management Experience.**
12. **Planning & Estimation of resources (human, tools, licences & Infrastructure)**
13. **Procurement of the needed tools, equipment & infrastructure setup.**

## Skills:

### ASIC/Chip-Design:

1. *Architecture, Requirements and Chip-Definition.*
2. *Front-End ASIC:* VCS, NC-Verilog, Design-Compiler, RTL compiler, PrimeTime
3. *Verification:* Specman, Chrysalis, System Verilog OVM.
4. *Backend ASIC:* Apollo, Physical Compiler, Star-XT
5. *Programming Languages:* Verilog, C, C++, Assembly 8086
6. *Scripting:* Perl, Csh, Scheme, JavaScript, PHP, ActionScripts.
7. *Custom Design:* Cadence Schematic Composer, **Spice**.
8. *FPGA:* Xilinx ISE Foundation Flows & design Methodology
9. *Others:* **IPC in C++** etc.
10. *Env:* Solaris, Linux, Windows
11. *Standards:* H264, MIPI CSI/DPHY, Aurora, Ethernet, SOC Components, TN
12. Matlab , LABVIEW, COMSOL-MULTIPHYSICS

## Experience Details:

1. Infinera India Pvt Ltd (December 2017 – Present)
2. Mobiveil India Pvt Ltd (January 2014-September 2017)
3. Infinera India Pvt Ltd (June 2013 – December 2014)
4. University of Southampton, UK ( 2012 – 2013)
5. Rockwell Automation ( 2010- 2011)
6. Ikanos Communications ( 2009- 2010)
7. Manthan Semiconductors ( 2008- 2010)
  - Worked for NXP Semiconductors & Ikanos Communications
  - Manthan team was acquired by Ikanos Communications.
8. SimpleTech WTC Pvt Ltd (Founder/CEO) (2007 – 2008)
  - ASIC Design/Verification Consultancy
    - Aftek's Elven Microcircuits, Prodigy Labs and other small firms
  - Multiple Web / Social Products developed.
9. Nvidia Graphics (2006 )
10. Analog Devices (2001-2005)

## **Project Details (ASIC Design/Verification):**

### **Infinera India Pvt Ltd:**

December 2017-Present

Chip Architect, Design Lead, Chip Integration & Device Software. I am now working as Architect since last 4 years, driving the definition of current and next generation of Optical Networking Chips for Infinera. Before that I had dual role as Architect and Design Lead on the Communications Path on the Optical Networking Chip. In 2017, I was responsible for Sub-System Integration & Device Software.

Responsible for:

- Architecture, Requirements & Chip Definition.
- Design Lead for On Chip Mgmt. Communication System, -- used in multiple generations of Infinera Chip including the current and foreseeable future ones.
- Chip Integration & Device Software Development. (Past).

### **2020-2024:**

#### **Architect & Chip Definition:**

As Chip Architect, my role is to interact with Product-line marketing, keep up with latest Industry Standards (IEEE, ITU-T, OIF) in the Optical & Networking Space, make engineering judgement calls, develop & document requirements to define the Current and Next Generation of Infinera chips. These chips typically handle 800+ Gbps data and are used in the backbone networks. I am also involved in reviewing micro-architecture, design and verification plans, strategies and Test plans.

I have been involved in definition of ICE-X family of chips, which is available now to customers. There are other chips in pipeline. Together, I have been involved in definition of 4 chips.

Additional responsibilities include, making proposals to up-coming standards in Industry bodies- We have been making contributions to OIF for 1.6T transport.

### **2018-2020:**

#### **Architect & Design Lead:**

Defined the com-channel system for ICE-X family. Com-Channels in Optical Network chips are pathways, outside (and sometimes inside) of Datapath, on which control and management information flows. These could go as additional Ethernet stream with a different VLAN-ID, on Overhead fields of OTN frames, or just as out-of-band signals. All of these were built into a uniform structure and protocol stack. I was chief architect who conceptualized this system. Further, I was the Design-Lead to implement this. This also included hands-on work and the RTL was made fully configurable, so that it can scale with minimum resources across chip families. Being Arch and Design Lead, I was also involved in Oversight and review of verification, synthesis, STA, power analysis, Lint, CDC etc..

### **2017-2018:**

#### **Lead Integration, Software Development & subsystem documentation:**

I was responsible for documenting one of the three large sub-systems and integrating it. I was also responsible for Device Level software development for the sub-system which would integrate

easily into the SDK. The same API was used in Verification. This chip is now very successful in the marketplace as ICE-6 family from Infinera.

**Mobiveil India Pvt Ltd:**

January 2014-September 2017

Engineering Manager/SSD Architect, responsible for complex high performance SSD controller. Expected throughput exceeds 1M IOPs on random reads and writes for ASIC implementation. Team size 10.

Responsible for:

- Architecture
- Design & FPGA Implementation,
- Hardware Software partitioning.
- Board Bring up and Performance Enhancements.
- Overseeing Verification.

Also involved hands-on in a number of design modules, verification & scripting for improved efficiency.

Mobiveil has developed a product-line in SSD with two distinct architectures- The hardware accelerated one and Firmware Driven one. I have been responsible for both, as Engineering Manager/ Architect for the Hardware-Accelerated and for Firmware Driven SSD. A working Proof of Concept with 110+ kIOPs has been delivered to customers on Altera Arria-10 platform. A complete Architecture for firmware /processor driven SSD with NVMe accelerator engine has been developed.

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**Infinera Pvt Ltd. (Consultancy)**

June 2013 – December 2014

Bangalore, India

Design Consultant – Infinera is in long haul optical networks using OTN standards for network management. Since some of this is Infinera proprietary information, finer details cannot be disclosed. Work mostly relates to the optical frame management inside the Infinera network using the Infinera specific proprietary frame formats.

**University of Southampton:**

Sept 2011 – January 2013

M.Sc and then worked as an visiting researcher in Prof Hywel Morgan's Hybrid-Biodesives laboratory. Research focused on novel sensors using Impedance spectrometry. The work at an implementation level involved systems using FPGAs to process the sensor data and control the sensor operation. I was also responsible for evaluation & procurement of test & measurement equipment.

**Rockwell Automation. (Consultancy)**

April 2010 – September 2011

Bangalore, India

Independent Consultant - As a Design Verification Consultant with System Verilog / OVM verification environment.

**Senior Staff Engineer****Ikanos Communications**

August 2009 – August 2010

Bangalore, India

Ikanos Communications, (August 2009 to August 2010), Senior Staff Engineer., Part of this period as a consultant from Manthan Semiconductors (Aug 2009 - Nov 2009)

1. Lead and managed the delivery of Ethernet Sub-system. Included multiple designers & primary responsibility was technical leadership and co-ordination.
2. Led effort to speed up full chip verification environment with a group of 9 senior verification & design engineers.
3. Automated complete system-level verification environment completely from the running the tests running to results collection for the Ikanos GateWay Chip (15+ Million Gates). The automation of the environment was done using Perl/Csh scripts within make flow. It additionally used PhP scripting for some critical result collection/data analysis
4. Designed & Developed an Verilog/Perl based block level verification environment for Centralized DMA controller interfaced with three custom buses, and interacting with 10 different peripherals apart from memory & processor, together with their bus functional models
5. Supported and helped to fill gaps in the Specman/E block level environments for some critical components of the project.

6. Designed Ethernet header parser to extract information from the Ethernet packet to aid the software process it further. I also did associated DMA module, top-level re-organization and integration of the Ethernet port.
7. Designed Hash Engine for dynamic Indexed Routing

### **Member of Technical Staff at Manthan**

#### **Consultant @ NXP Semiconductors through Manthan SemiConductors**

May 2008 – June 2009

Bangalore, India

NXP Semiconductors through Manthan Semiconductors (May 2008 - June 2009) Consultant at NXP, Member of Technical Staff at Manthan.

1. Proposed architecture for a display router chip at NXP. Worked with Architects to freeze on the customer requirements in clear terms for designers.
2. Design of the DBI-Tx IP with support for TypeB, TypeC MIPI DBI- interface. Developed block level verification environment to test it before being tested at the system level by the verification team.
3. Top Level Integration of a Display Router Chip, which includes Analog integration, Power integration etc.
4. Design of MIPI Rx and MIPI Tx IPs with Digital portion of DPHY. Complete Architecture, design & verification plan implementation done. Environment again designed in Perl/Verilog.

### **Independent ASIC Design/Verification Consultancy:**

(Consultancy was undertaken along with other activities at SimpleTech WTC Pvt Ltd)

September 2006 – November 2008

Bangalore, India

1. Lead & Managed a team of 2 design and 5 verification Engineers to deliver MIPI CSI & DPHY Trans-receiver (Transmitter + Receiver) IPs to Elven Microcircuits (a venture of Atek Infosys, Pune). I was responsible for team and project management – up to net-list delivery of MIPI Rx and MIPI Tx IPs with Digital portion of DPHY. Complete Architecture, design & verification plan implementation done. Environment again designed in Perl/Verilog. Project done for **Elven Micro-circuits, Bangalore (division of Atek Infosys, Pune)**
2. Development of a high performance signal processing library in C, target for ARM processor, to compute STFT for a real time audio signal in a TRP application. Project done for **Prodigy Labs** & was focused on Algorithm development and Software coding.
3. Development of a network analyzer using C++, ethereal and inter-process communication for Brahmarshi **Technologies**.

### **Sr Design Engineer**

#### **Nvidia Graphics**

January 2006 – August 2006

Bangalore, India

Nvidia Graphics (Jan 2006 - Aug 2006), Sr Design Engineer

- RTL for H264 AVC integration in the encoder

### **Sr Design Engineer**

#### **Analog Devices**

January 2001 – September 2005

Bangalore, India

1. Designed a centralized DMA controller with 12 peripheral & 4 Memory channels for a high end DSP processor. Design included design of 3 proprietary bus interface designs.
2. Designed PCS layer of a high speed peripheral block, (Xilinx AURORA Trans-receiver).
3. Developed a scalable verification environment in Perl/XML for DMA controller verification.
4. Developed configurable BFMs as a verification component for DDR II controller & 4-way Set associative cache.
5. Developed a Back end flow for automated clock tree synthesis & routing. Evolved & Automated the entire back end flow for 0.13u Technology
6. Developed Cad Automation for hold fix.
7. Developed a Specman based automatic test generator for state machine testing.

### **Education:**

#### **University of Southampton, Southampton, UK**

Aug 2011 – Sept 2012

M.Sc. Electrical Engineering, Nanotechnology 80%

Top 2% in cohort of 400 students (all M.Sc. together)

#### **Karnataka University, Dharwad, India**

Oct 1996 – Nov 2000

Bachelor of Engineering Electronics & Communications 84.33%.

(Top 2% in the University)

#### **Visiting Researcher**

Sept 2012 – January 2013

Hybrid Bio Devices Laboratory, with Prof Hywel Morgan's Lab.

### **US Visa/Work Permit Information:**

**US B1/B2 – Till 2034.**