

## **Anand J. Bariya, PhD**

301, Supra Homes, Nehrunagar, Near Water Tank, Off Gokul Road, Hubli 580030  
+91-98865-06025 | abariya@alumni.stanford.edu

**Outcome-oriented leader with exemplary track-record in building effective teams, nurturing talent and forging impactful partnerships. Execution focused. Creative and resourceful in defining, developing and delivering skill-development programs that meet challenging industry requirements. Motivated by the transformative power of appropriate educational interventions in driving social and economic development.**

### **EDUCATION**

**PhD** Stanford 1990 | **MS** Stanford 1987 | **BTech** IIT Bombay 1985

### **INDUSTRY EXPERIENCE**

**Tata Consulting Services (06/2023 – present)**

#### **Senior Industry Advisor**

- Define and execute strategy for growing TCS' nascent practice in semiconductor engineering services. Build internal capability and external partnerships.
- Establish academic partnerships with universities for talent development in advanced IC packaging

**SiFive Inc. (08/2018 – 04/2023)**

#### **Senior Vice President and Managing Director, India Operations, Bangalore**

- General management of the custom silicon business unit, including engineering, pre-sales, IT, procurement and customer contracts. Built and oversaw 150-person engineering and IT organization with broad capabilities in IC design and embedded software development, and global IT support.
- Implemented Apprenticeship and Traineeship programs for freshers with diploma or BSc degrees, expanding sourcing of fresh talent to non-BTech cohorts.

**Broadcom (03/2012 – 06/2018)**

#### **Senior Director, Bangalore, India**

(Broadcom acquired NetLogic in 2012.)

- Drove the complete design and productization of large integrated circuits manufactured at advanced technology nodes
- Recruited and nurtured talent for all critical engineering and support functions
- Established and drove successful program for identifying, onboarding and training fresh college hires from tier-3 colleges across India

**NetLogic Microsystems (01/2005 – 03/2012)**

#### **Vice President and Managing Director, India Operations, Bangalore**

- Established design center from scratch and grew it to over 120 professionals in engineering, IT and general administration.
- Defined HR and compensation policies, drove recruitment, managed legal and regulatory compliances, and oversaw facilities & infrastructure.

**Toshiba America Electronics (04/2002 – 01/2005)**

#### **Senior Manager, ASIC Design Center, San Jose, CA**

- Managed all aspects of ASIC design and delivery, including customer and factory interfaces.
- Drove business development and sales efforts to secure design wins.

**Vitesse Semiconductor Corp. (2000 – 2002)**

#### **Design Integration Manager, Santa Clara, CA**

- Drove implementation of advanced network processor silicon.

**Cadence Design Systems Inc. (1998 – 2000)**

#### **Senior Technical Marketing Manager, San Jose, CA**

- Responsible for technical marketing and product engineering of interconnect extraction and signal integrity tools. Defined market requirements and detailed product specifications.

**National Semiconductor Corp. (1990 – 1997)**

#### **Staff Process R&D Engineer, San Jose, CA & Design Manager, India Design Center, Bangalore, India**

- Managed SoC design team to support international design projects initiated in Israel or Santa Clara. Led team in design implementations from synthesis through tape-out.

- Developed and implemented employee training and mentoring process. Managed academic interactions and third-party R&D collaborations. Initiated and managed student co-op program.
- of 0.8, 0.65 and 0.45 um CMOS technologies, including process integration, design rule definition, test chip design, data analysis, yield analysis, SPC, WIP control, process split implementation, documentation, qualification and technology transfer.

## ACADEMIC/TEACHING/SKILL-DEVELOPMENT EXPERIENCE

### Deshpande Foundation (04/2023 – present)

#### Chief Executive Officer

- Developed and launched skill-development programs for high-paying entry-level jobs in investment banking, business process automation, pharmaceuticals and IT services. Program beneficiaries are rural, BPL graduates. Program delivery is in residential facilities in Hubli, Karnataka & Nizamabad, Telangana, as well as on-site in colleges across North Karnataka, Telangana and Marathawada (Maharashtra).
- Drove development and delivery of content for English proficiency, computing and mathematical capability.
- Identified and onboarded training partners for Investment Banking Operations and Full-Stack Development. Established Social Impact partnership with Coursera.
- Defined, developed and implemented a “Vocational Livelihoods” program with corporate partners.

### KLE Tech University, Hubli

#### Visiting Faculty and Advisor

- Ran faculty development programs in the areas of Semiconductor Technology and IC Design
- Organized workshops on RISC-V architecture and while at SiFive
- Drove development and delivery of project-based, hands-on courses in IC Design
- Established industry partnerships with Mentor Graphics and Cadence Design Automation
- Established program in Advanced IC Package Design in partnership with TCS. Program involved semester-long student internships and development of elective courses.

### IIIT-Bangalore

#### Visiting Faculty

- Developed and delivered course on IC Design collaboratively with senior member of full-time faculty.

### Ahmedabad University (01/2014 – 12/2014)

#### Senior Consultant, School of Engineering & Technology

- Functioned as interim director to get institute off the ground
- Defined curriculum and launched programs centered on project-based pedagogy
- Recruited technical staff and faculty
- Taught introductory course on IC Design.

### Intel India Electronics (1997-1998)

#### Academic Program Manager

- Initiated and established India Program for Intel’s Global Academic Program
- Established Intel Microelectronics Lab in IIT-Bombay. Defined and funded research project in interconnect extraction.
- Established Intel Enterprise Laboratory in IIM-Bangalore

### University of California Santa-Cruz (2000 – 2003)

#### Course Developer and Instructor, Extension Program

- Developed and taught course on ASIC Design in UCSC Extension.

## AND FINALLY...

- General Chair, IEEE 12th International Conference on VLSI Design, January 1999.
- Authored or co-authored over 8 papers in conference proceedings and peer-reviewed journals
- Holder of patent (US 5443941 A) for a plasma polymer antireflective coating for photolithography.